

REMARKS

The Office has objected to Figures 2 and 3 because of improper cross-hatching. The Office has rejected claims 1-3, 5-8, 17, 19, and 20 under U.S.C. § 103(a) as being unpatentable over Harada (6,198,362) in view of Klaser (4,870,746) and Archambeault (6,418,031).

Drawings Objection

Applicant is submitting corrected drawings (Figures 2 and 3) with this reply. These figures now include proper cross-hatching throughout. Also, the via holes in pad 165 of FIG. 3 are now shown with a different hatching pattern to make them stand out from the pad itself.

The 103(a) Rejection

Three fundamental tenets of the law of obviousness are at issue here. First, "a prior art reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 31 USPQ2d 1130 (Fed. Cir. 1994). Second, even when it might be true that a prior art structure could be modified to form the claimed structure, "the mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Laskowski*, 10 USPQ2d 1397 (Fed. Cir. 1989). Third, "it is impermissible . . . simply to engage in hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps." *In re Gorman*, 18 USPQ2d 1885 (Fed. Cir. 1991).

Harada fails to show or suggest "a loss element residing in an internal layer of the circuit board and connected electrically between the power layer and ground layer to suppress electrical noise caused by changes in current flow in the circuit components," as the Office has conceded. This failure on Harada's part is not a mere oversight, however, but is the result of a specific teaching away from Applicant's structure. " Harada

specifies that the lossy elements be spaced along "at least two belt-shaped conductive loops on the periphery of the circuit board," for the purpose of preventing "an undesired electromagnetic wave . . . from radiating." (Col. 6, lines 20-22 and 43-45). In other words, Harada has carefully placed these components along the outer edge of an outer layer of the board to inhibit the propagation of unwanted electromagnetic waves away from the board. Applicant, on the other hand, has discovered that a better solution is to attempt to prevent the existence of such waves in the first place and does so by embedding the lossy elements within the circuit board. Harada's carefully selected placement of these components in a ring formation around an outer edge of an outer layer of the board would lead a person of ordinary skill away from, not toward, a solution like Applicant's.

What's more, neither one of the other references cited -- Archambeault and Klaser -- offers any suggestion or motivation to move these particular components from the outer layer of Harada's board to the inner layers. Neither of these references is even aware of the problems that Harada and Applicant were tackling, and therefore neither could possibly suggest the desirability of modifying to Harada's component-placement technique. In defending its use of these references, the Office urges that the person of ordinary skill would naturally know to move Harada's components into the circuit board for the purpose of saving space. This argument, however, misses the point. Space savings is not the issue in Harada; mitigating the effects of EM interference is. Confusing these two issues would, if anything, render Harada's solution less effective, not more so. In any event, neither Archambeault nor Klaser provides any motivation to make such changes to Harada.

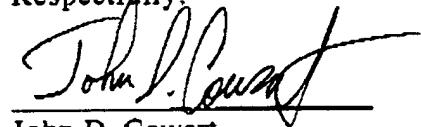
It is clear that the Office's only motivation for combining these three references is an improper hindsight reconstruction of the claims using Applicant's specification as a guide. Applicant does not dispute that embedding circuit components within a board, as shown in Klaser, is well known. But embedding the specific type of components of interest here is not known, and doing so is not an obvious extension of the teachings of these references. There is simply nothing in any of these references that would lead a person of ordinary skill to believe that one should or even could move the lossy elements from the outer edge of Harada's board into the internal layers.

CONCLUSION

The Harada, Archambeault, and Klaser references cannot be properly combined to construct Applicant's invention. Even if they could be combined, these references would not show or suggest the invention. Therefore, all of Applicant's claims are allowable over these references.

Applicant asks the Examiner to reconsider this application and to allow all of the claims. Please apply any charges that might be due, excepting the issue fee but including fees for extensions of time, to deposit account 50-1673.

Respectfully,



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Invention Title: Introducing loss in a power bus to reduce emi and electrical noise
Inventor: R. Alexander
Serial No.: 09/752,352

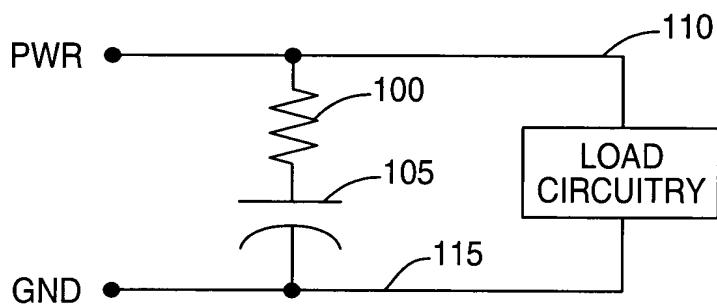


FIG. 1

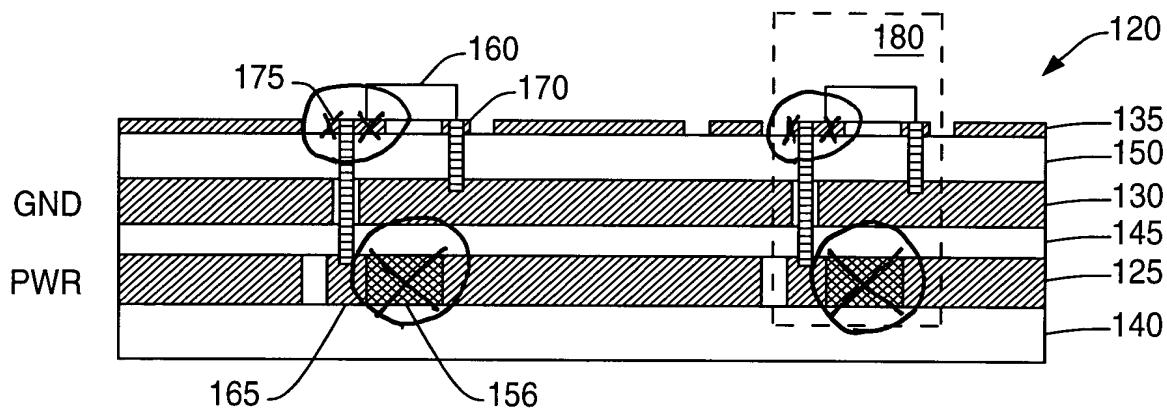


FIG. 2

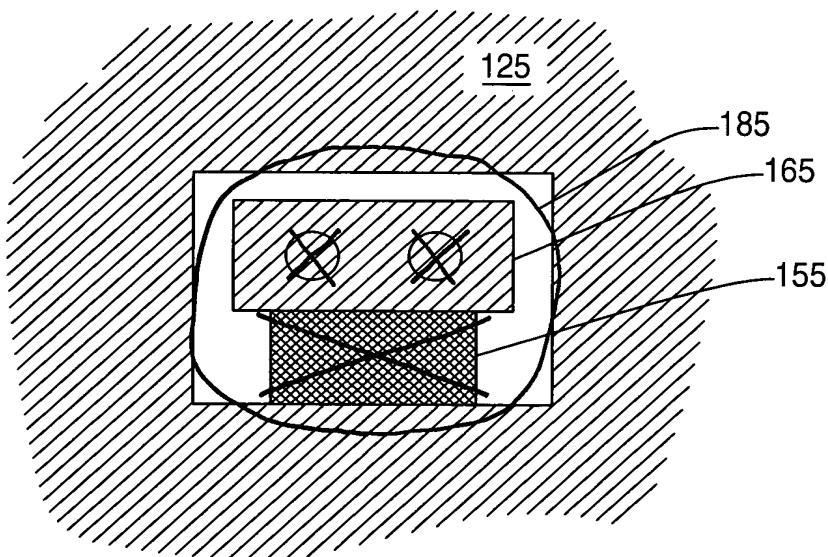


FIG. 3

(SEE ATTACHED SHEET)

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Inventor: R. Alexander
Serial No.: 09/752,352

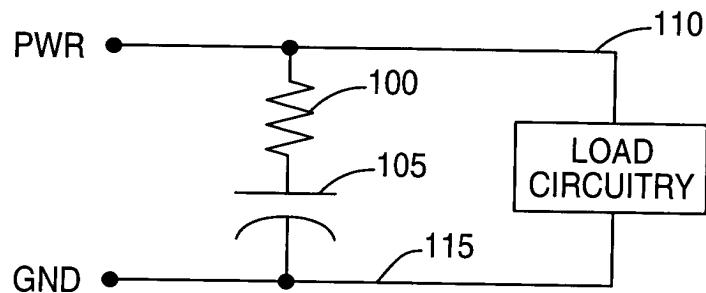


FIG. 1

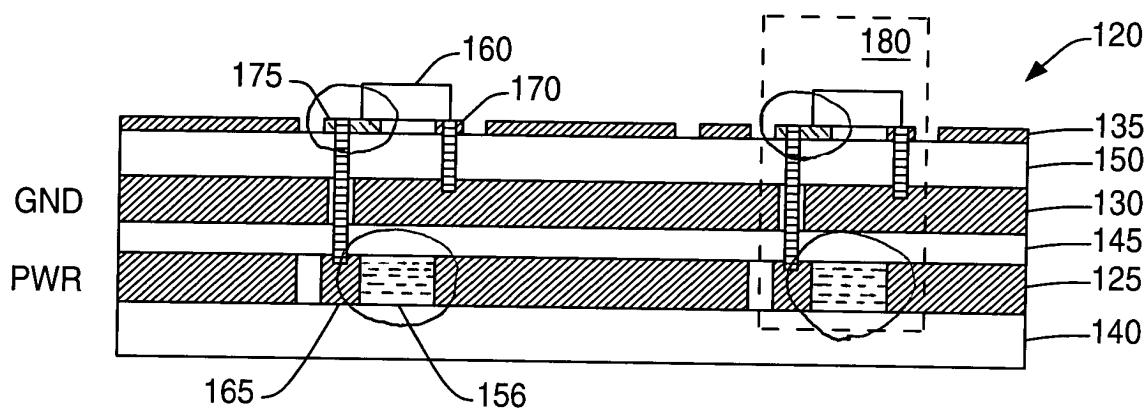


FIG. 2

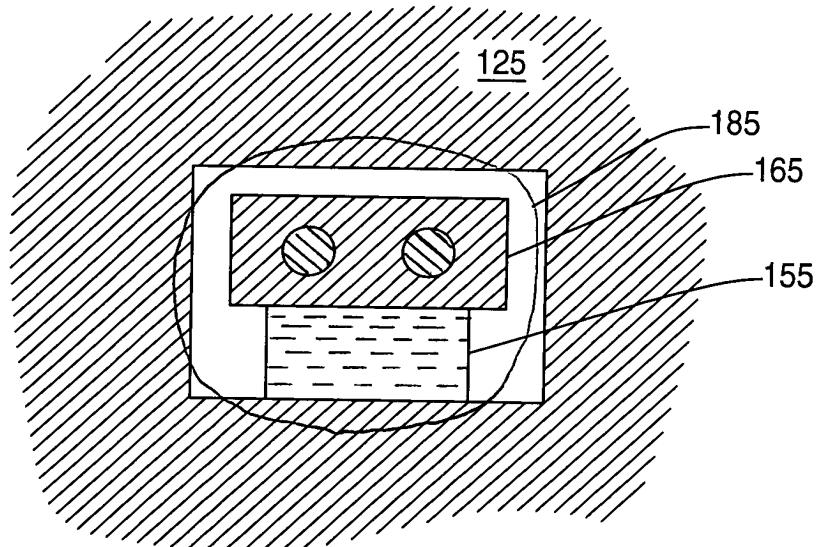


FIG.3

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Inventor: R. Alexander
Serial No.: 09/752,352

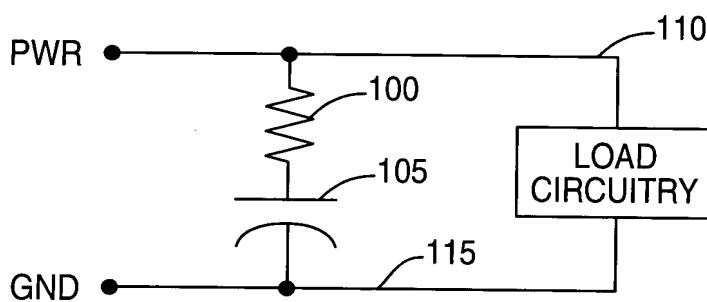


FIG. 1

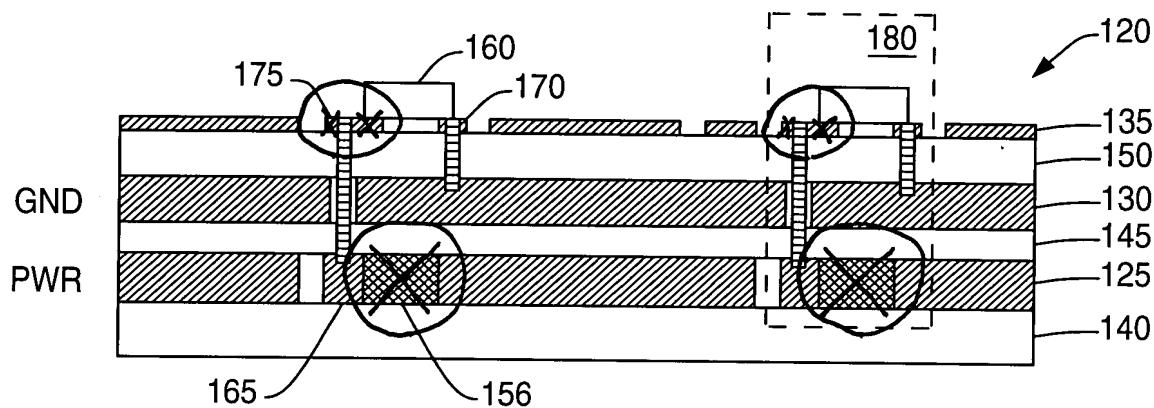


FIG. 2

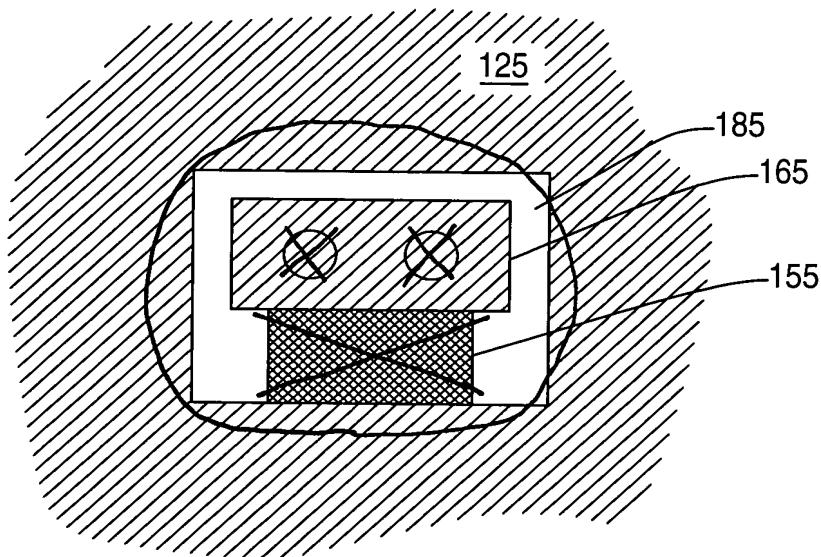


FIG. 3

(SEE ATTACHED SHEET)

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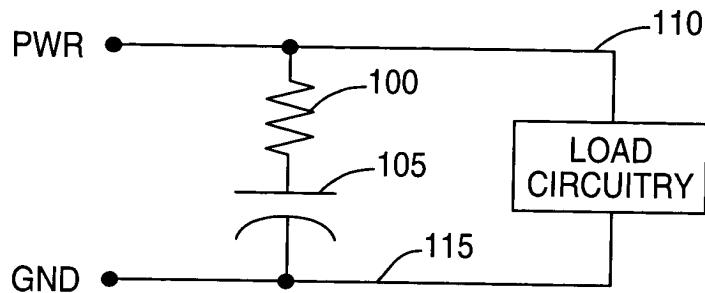


FIG. 1

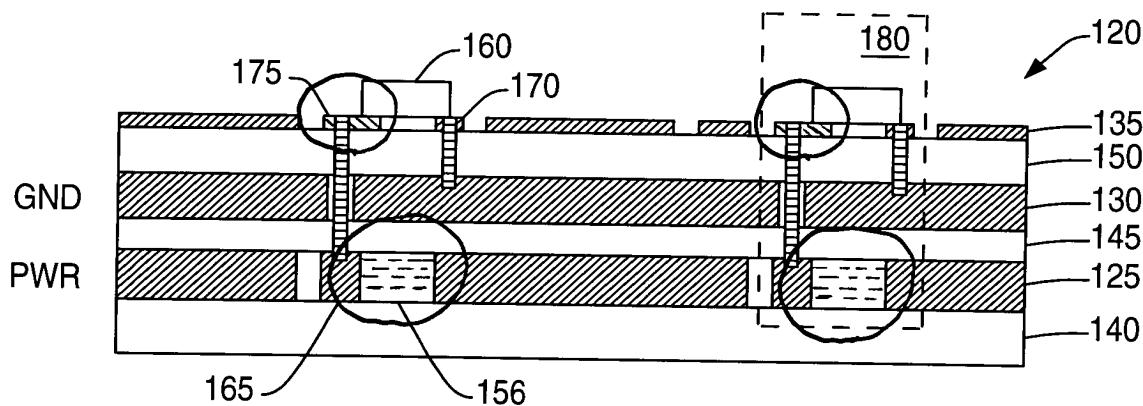


FIG. 2

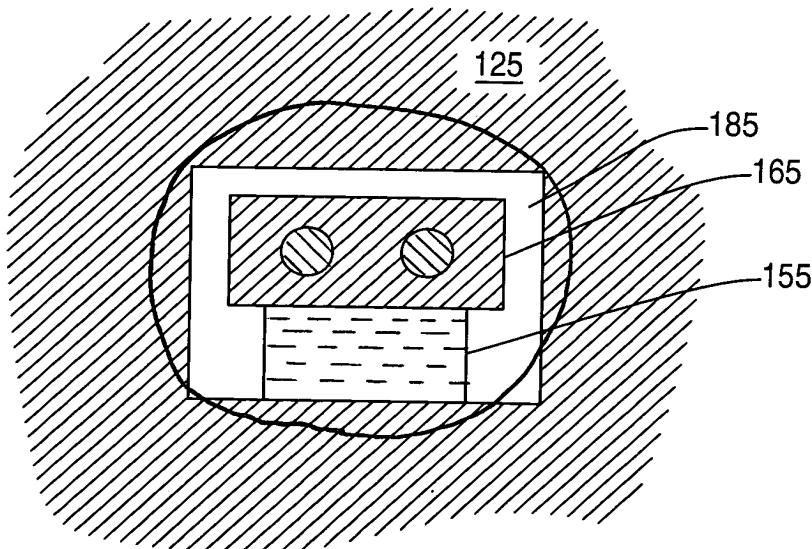


FIG. 3